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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/003,857 | 11/02/2001 | David B. Fox | POU920010048US1 | 7451 |

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| EXAMINER | |
|---|---|
| CHACE, CHRISTIAN | |
| **ART UNIT** | **PAPER NUMBER** |
| 2187 | 6 |

DATE MAILED: 07/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/003,857 | FOX ET AL. | |
| | Examiner | Art Unit | |
| | Christian P. Chace | 2187 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *05 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7 and 18* is/are allowed.

6)☒ Claim(s) *1-6 and 8-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

This Office action has been issued in response to amendment filed 5 April 2004. Claims 1-18 are pending. Claims 7 and 18 are allowed. However, even in light of the instant amendment, claims 1-6 and 8-17 are rejected, as detailed below. Accordingly, this action has been made FINAL, as necessitated by amendment.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 8, 10, and 13-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Assouad et al (US Patent #6,119,254).

With respect to independent claim 1, a method of allocating a trace array from a cache memory is disclosed in column 2, lines 62-64. A trace array is a dedicated section [of a memory] allocated for trace data, and a data buffer is a cache.

In a system mode, using all of the cache memory as a data cache, and in a trace mode, dividing as follows, is disclosed in column 2, lines 58-60, which recite, "The tracing buffer memory of the present invention is a section of the data buffer memory normally used for the target product's normal operations."

Dividing said cache memory into a reduced-size cache memory and a trace array is disclosed in column 2, lines 62-64. If a cache is divided, one part is inherently going to be smaller than the original whole, as can be seen in figure 6, for example.

Permitting storage of trace signal data into said trace array is also disclosed in column 2, lines 62-64.

Permitting retrieval of said trace signal data from said trace array is disclosed in column 12, lines 28-30.

With respect to claim 3, said reduced-size cache memory not being equal in size to said trace array is disclose din figure 6 as well, which shows the trace array being 1/3 the size of the R/W function area of the buffer/cache.

With respect to claim 8, detecting a trace mode is disclosed in the abstract in lines 3-5, specifically.

With respect to claim 10, the combination of said reduced-size cache memory and said trace array comprising a split cache spanning the addressable space of said cache memory is, again, shown in figure 6, and further discussed in column 9, lines 15-40. Again, the cache is split into a R/W function area and a Trace Array area.

With respect to claim 13, the reduced-size cache memory and the trace array being each associated with a separate output bus is disclosed in column 2, lines 40-45, where each data port is an output bus. Also, see figure 4, where tracing data FIFO has separate bus 304 into gate 402, where microprocessor data FIFO (cache data FIFO) has bus 443 into gate 403.

With respect to claim 14, characterizing a self-timed interconnect using said trace array is disclosed in column 8, lines 27-30. (Examiner also wishes to note that a self-timed interconnect is admitted prior art in paragraph [0023] of the instant specification as well.)

Switching back to the original cache functionality once characterization is complete is disclosed in column 12, lines 53-56.

With respect to claim 15, at least one of multiplexing and time-sharing said self-timed interconnect signals with other signals to be stored in the trace array is disclosed in column 8, lines 5-6, which discloses multiplexing the signals to be stored in the trace array.

With respect to independent claim 16, a storage medium encoded with a machine-readable computer program code for allocating a trace array from an original cache memory, said storage medium including instructions for causing a computer to implement a method [for allocating a trace array from a cache memory] is disclosed in the abstract as programmed tracing circuitry.

In a system mode, using all of the cache memory as a data cache, and in a trace mode, dividing as follows, is disclosed in column 2, lines 58-60, which recite, "The tracing buffer memory of the present invention is a section of the data buffer memory normally used for the target product's normal operations."

Dividing said cache memory into a reduced-size cache memory and a trace array is disclosed in column 2, lines 62-64. If a cache is divided, one part is inherently going to be smaller than the original whole, as can be seen in figure 6, for example.

Permitting storage of trace signal data into said trace array is also disclosed in column 2, lines 62-64.

Permitting retrieval of said trace signal data from said trace array is disclosed in column 12, lines 28-30.

With respect to independent claim 17, a computer data signal for allocating a trace array from an original cache memory, said computer signal comprising code configured to cause a computer to implement a method [for allocating a trace array from a cache memory] is disclosed in the abstract as programmed tracing circuitry.

In a system mode, using all of the cache memory as a data cache, and in a trace mode, dividing as follows, is disclosed in column 2, lines 58-60, which recite, "The tracing buffer memory of the present invention is a section of the data buffer memory normally used for the target product's normal operations."

Dividing said cache memory into a reduced-size cache memory and a trace array is disclosed in column 2, lines 62-64. If a cache is divided, one part is inherently going to be smaller than the original whole, as can be seen in figure 6, for example.

Permitting storage of trace signal data into said trace array is also disclosed in column 2, lines 62-64.

Permitting retrieval of said trace signal data from said trace array is disclosed in column 12, lines 28-30.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Assouad et al as applied to claims 1, 3, 8, 10, and 13-17 above, and further in view of Kirk (US Patent # 5,875,464).

With respect to claim 2, Assouad et al disclose the subject matter discussed supra with respect to claim 1, upon which the instant claim depends.

The difference between the instant claim and Assouad et al is the explicit recitation that the reduced-size cache is equal in size to the trace array.

However, Kirk discloses partitioning a cache in halves (where both partitions are equal) in column 15, lines 30-33.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Assouad et al and Kirk before him/her, to utilize the equal partitions of Kirk in the system of Assouad et al because this technique minimizes the required hardware, as disclosed by Kirk in column 15, line 37. In addition, Assouad et al in column 1, lines 65-67, discuss the development of single-chip technology, which requires as much reduced hardware as possible to reduce the size of the required single chip and thereby increase the speed.

where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device."

With respect to claim 5, Assouad et al disclose the subject matter discussed supra with respect to claim 1, upon which the instant claim depends.

The difference between the instant claim and Assouad et al is the explicit recitation that at least one of said cache memory and said reduced-size cache memory is organized into eight-way associativities.

Kirk discloses eight-way associativity partitioning in column 12, line 46.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Assouad et al and Kirk before him/her, to utilize the eight-way associativity of Kirk in the system of Assouad et al because it can provide significantly better performance, as disclosed by Kirk in column 12, lines 50-51.

With respect to claim 6, Assouad et al disclose the subject matter discussed supra with respect to claim 1, upon which the instant claim depends.

The difference between the instant claim and Assouad et al is the explicit recitation that the cache memory comprises a directory array.

Kirk discloses a TLB, which in MIPS R3000, includes an on-chip TLB as disclosed by Kirk in column 19, line 52 and also in column 20, lines 19-24.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to utilize the TLB of Kirk in the system of Assouad et al, because

the MIPS R3000 system (which contains the TLB as discussed supra) provides support for hierarchical memory design to provide high memory bandwidth necessary to run without pipeline stalls, as discussed by Kirk in column 20, lines 41-45.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Assouad et al as applied to claims 1, 3, 8, 10, and 13-17 above, and further in view of Fischer et al (US Patent #6,376,358).

Assouad et al disclose the subject matter discussed supra with respect to claim 1, upon which the instant claim depends.

The difference between the instant claim and Assouad et al is the explicit recitation that the cache memory is comprised by a system-on-chip environment.

Fischer et al disclose a system-on-chip environment in column 1, line 18.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Assouad et al and Fischer et al before him/her, to utilize the system-on-chip environment of Fischer et al in the system of Assouad et al because the system-on-chip environment has faster speed and overcomes bandwidth and capacitance problems associated with off-chip connections, as discussed in column 1, lines 19-21 of Fischer et al.

***Allowable Subject Matter***

Claims 7 and 18 are allowed.

***Response to Arguments***

With respect to applicants' argument that claims 11 and 12 are, indeed, enabled by the specification, examiner agrees solely in light of applicants' discussion on page 6

of the instant remarks, which offers a clearer discussion than the instant specification. Accordingly, the 35 USC 112, 1st Paragraph rejection has been removed.

With respect to applicants' argument that Assouad does not disclose a system mode and a trace mode a claimed in the instant amendment, examiner respectfully disagrees, and refers applicants to column 2, lines 57-60, which are discussed supra with respect to the independent claims upon which they apply. "normal operations" is "system mode" and tracing buffer" operations is "trace mode."

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian P. Chace whose telephone number is 703.306.5903. The examiner can normally be reached on 9-4-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703.308.1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christian P. Chace
DS/cpc

DONALD SPARKS
SUPERVISORY PATENT EXAMINER